Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph starting at **page 9, line 36**, with the following rewritten paragraph:

~~Fig. 57 shows~~ Figs. 57(a), 57(b), and 57(c) show the overall structure of a memory 10 system according to an eleventh embodiment of the present invention.

Please replace paragraph starting at **page 10, line 16**, with the following rewritten paragraph:

~~Fig. 65 is a diagram~~ Figs. 65(a) – 65(h) are diagrams showing combinations of write data WD and verify data VD.

Please replace paragraph starting at **page 10, line 18**, with the following rewritten paragraph:

~~Fig. 66 illustrates~~ Figs. 66(a) – 66(c) illustrate the distribution of potential levels after the verify operation and the dependency of a bit line on the threshold value.

Please replace paragraph starting at **page 10, line 23**, with the following rewritten paragraph:

~~Fig. 68 is a diagram~~ Figs. 68(a) – 68(h) are diagrams showing combinations of write data WD and verify data VD.

Please replace paragraph starting at **page 10, line 25**, with the following rewritten paragraph:

~~Fig. 69 illustrates~~ Figs. 69(a) – 69(c) illustrate the distribution of potential levels after the verify operation and the dependency of a bit line on the threshold value.

Please replace paragraph starting at **page 10, line 36**, with the following rewritten paragraph:

~~Fig. 74 shows~~ Figs. 74(a) – 74(c) show general circuits embodying the present invention.

Please replace paragraph starting at **page 11, line 5**, with the following rewritten paragraph:

~~Fig. 78 shows~~ Figs. 78(a) and 78(b) show a chip circuit diagram and a threshold value distribution graph according to an embodiment of the present invention.